On-Board Processor for Direct Distribution of Change Detection Data Products

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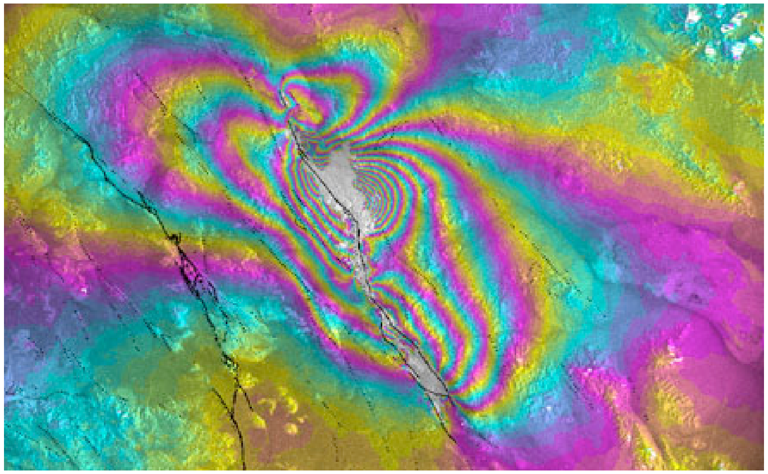
Outline

- Motivation for the Change Detection On-Board Processor (CDOP)
- Objectives of CDOP development
- Applications for CDOP
- Processor requirements
- Processor algorithm
- Processor architecture
- Status of processor development
- Summary

Motivation for Change Detection On-Board Processor

- The performance of many spaceborne synthetic aperture radar (SAR) mission concepts are limited by downlink data rate
  - e.g. An InSAR mission concept for JIMO requires 180 Mbps raw data downlink for two data channels. The JIMO spacecraft will currently accommodate a 10 Mbps downlink rate to the Deep Space Network. We need to compress the radar downlink rate by a factor of 18 or reduce performance (resolution, height accuracy, and/or swath).

- The utility of spaceborne imaging radars will be greatly enhanced if we can deliver useful data products to the end-users in a timely manner
  - e.g. Observation and use of surface deformation data over rapidly evolving natural hazards.



Surface deformation from an earthquake

Objectives of the CDOP Development

Develop an on-board imaging radar data processor for repeat-pass change detection and hazards management that features

- Real-time SAR image formation (FPGA-based)
- Real-time differential interferogram formation (microprocessor-based)
- Compact and flexible processor architecture

Provide a path to real-time, on-board processing for spaceborne imaging radar missions that will enable

- Near real-time observation of surface change due to flooding, forest fire, volcano eruption, and vegetation growth
- Near real-time observation of surface deformation due to earthquake, volcano eruption, glacier and sea ice movements
- Supply of vital information for natural disaster management
- Reduced downlink data rate

Relevance to On-Going/Future NASA Programs

CDOP will enable/enhance the following missions/mission concepts:

- Potential Spaceborne SAR Missions
  - EarthScope: L-band InSAR for Repeat-Pass Interferometry
  - JIMO:
    - Concept 1: P/S-band polarimetric SAR
    - Concept 2: Ka-band Single-Pass InSAR
  - Mars: P-band SAR
  - Moon: Low frequency SAR
- AIRSAR: DC-8 based P/L/C-band Pol/InSAR
  - Provide real-time high resolution SAR imagery
- UAVSAR: UAV-based L-band SAR for repeat-pass interferometry under development
  - Provide real-time high resolution SAR imagery
  - Provide near real-time change detection capability

Summary of CDOP Functional Requirements

- Able to ingest 8-bit or BFPQ data in either offset video or I & Q format in real time
- Able to range compress each pulse in real time
- Able to generate presummed data in real time
- Able to acquire position, attitude, radar waveform data in real time
- Able to support at least an 8-point interpolator for range migration correction
- Have sufficient throughput to simultaneously range compress and presum incoming pulse data while performing azimuth compression on the previous patch data
- Have sufficient I/O bandwidth to simultaneously access pulse data and to output final products to a display device and data storage device
- For airborne data, be able to motion compensate the data to a common reference line in real time prior to azimuth compression

Summary of CDOP Functional Requirements

Goals:

- Have sufficient throughput to process 2 channels simultaneously
- Able to generate filtered interferograms in real time
- Able to generate a correlation map in real time
- Able to generate differential interferograms corresponding to surface change in real time

Typical UAVSAR System Parameters

Parameters	Value
Range bandwidth	80 MHz
Sampling rate (offset video)	180 MHz
Pulse length	30 us
PRF	350 Hz
Wavelength	0.24 m
Antenna length	1.5 m
Range FFT Size	16384
Number valid range samples	7720
Range swath	16 km
Range pixel size	1.66 m
Azimuth resolution	0.75 m
Azimuth reference function	5850
Azimuth samples per patch	16384

Typical Spaceborne SAR System Parameters

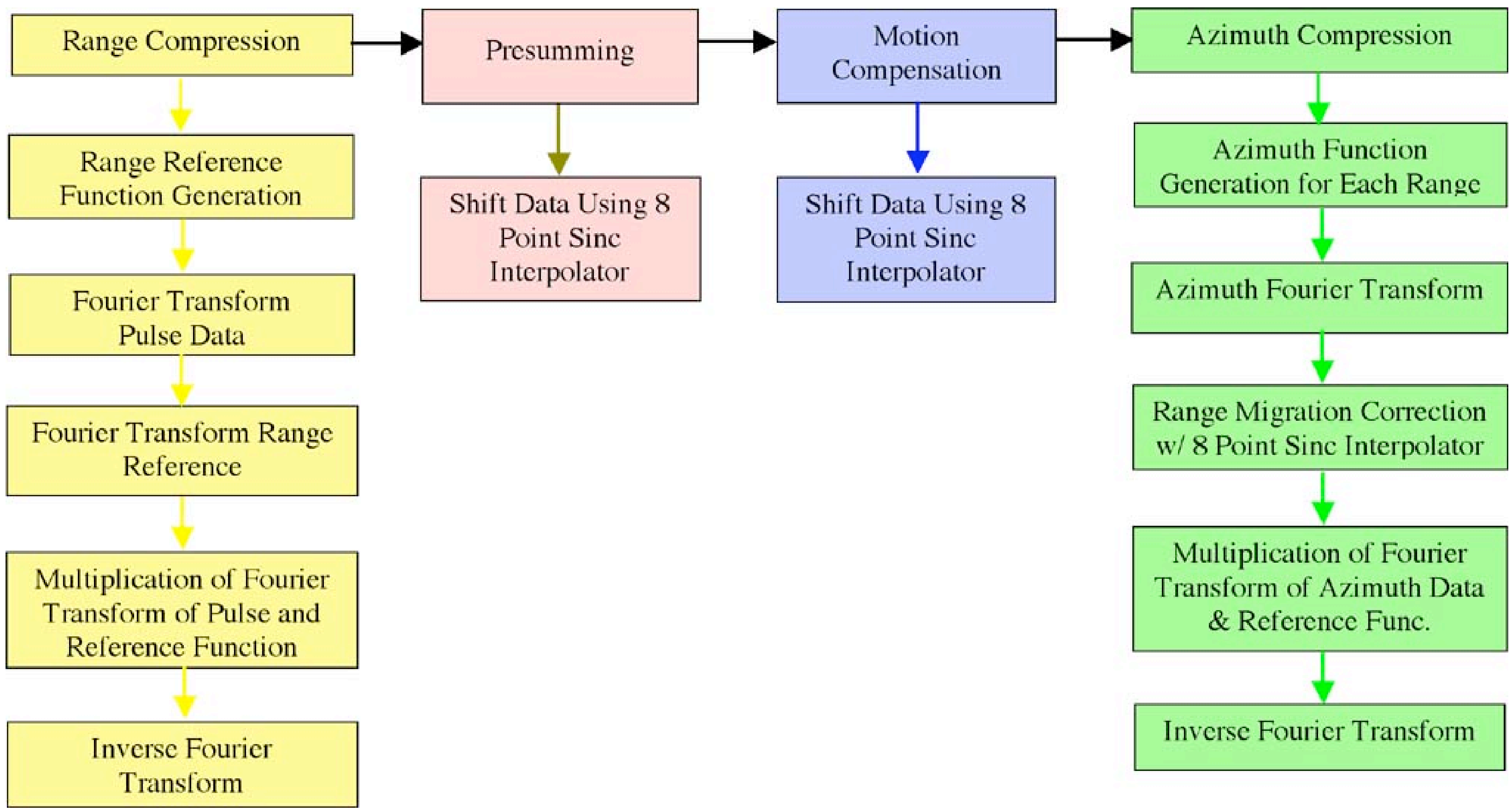
Assume European Space Agency's ERS C-band radar flown at 780 km in a 98° inclination angle orbit with look angle range from 17° to 23°

Parameters	Value
Range bandwidth	15.55 MHz
Sampling rate (IQ)	18.96 MHz
Pulse length	37.1 us
PRF	1679 Hz
Wavelength	0.056 m
Antenna length	12 m
Range FFT Size	8192
Number valid range samples	6000
Range pixel size	7.9 m
Azimuth resolution	2.9 m
Azimuth reference function	1024
Azimuth samples per patch	8192

Summary of CDOP Performance Requirements

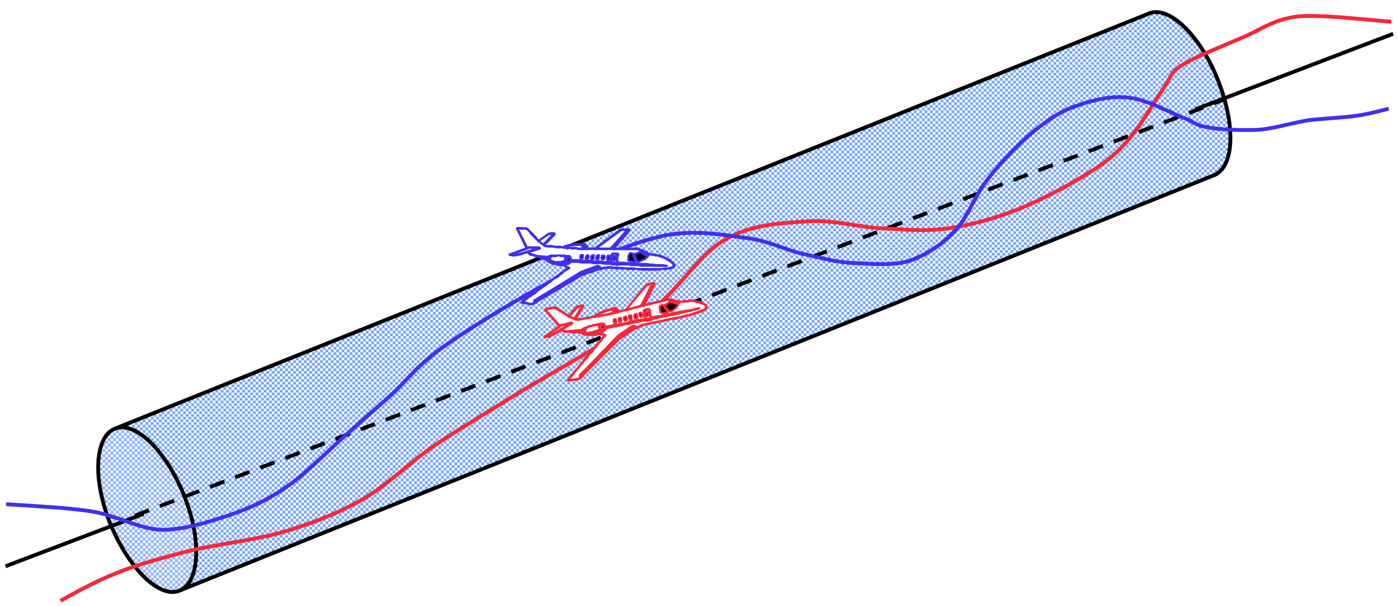
- FPGA throughput (airborne/spaceborne): 2/11 GFLOPS
- Microprocessor throughput (airborne/spaceborne): 0.2/2 GFLOPS
- Internal data rate:
  - 400 Mbps for the FPGAs
  - > 2 Gbps from microprocessor to disk
- Memory:
  - 1 GB for each FPGA board
  - 4 GB for the microprocessor board
- ISLR: < -12 dB
- Phase noise induced by the processor: < 1°

Flow Diagram of SAR Image Formation

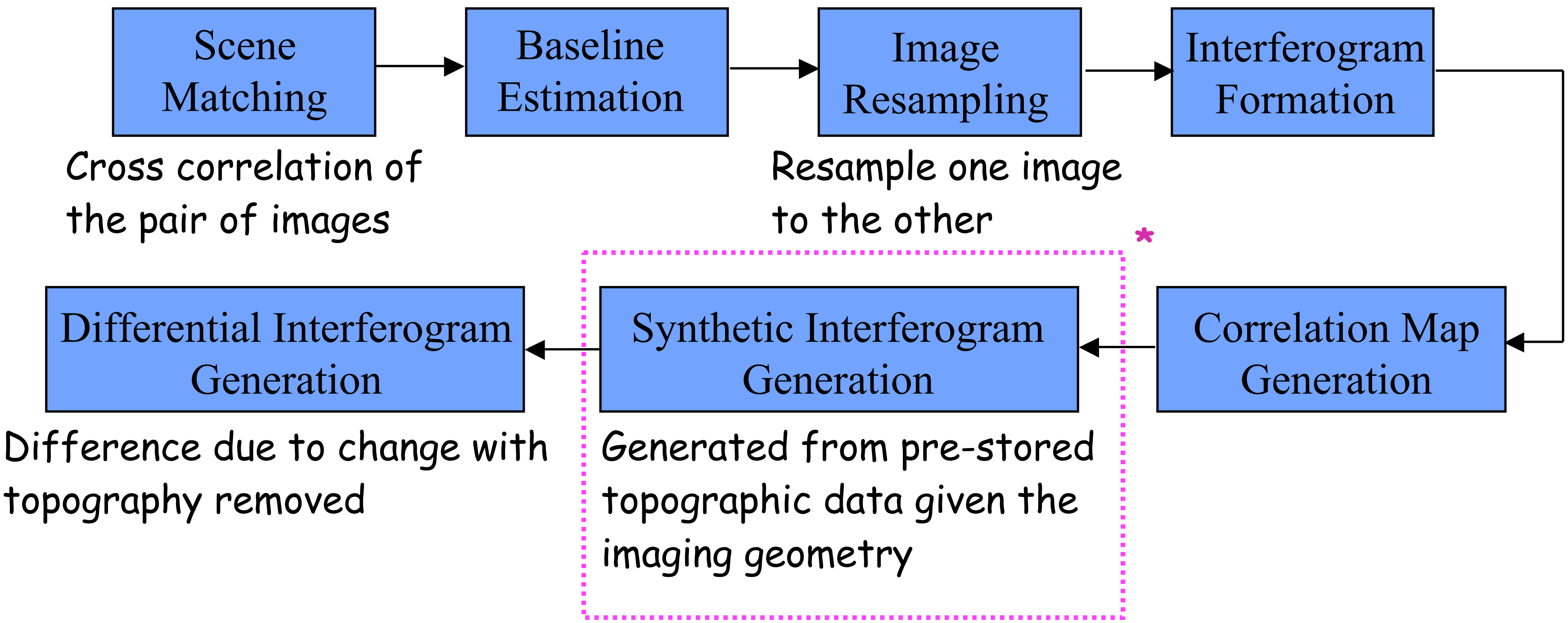


Importance of Motion Compensation

- Motion compensation is the process where the radar signal data are resampled from the actual path of the antenna to an idealized path called the reference path
- Motion compensation is necessary in airborne single-pass or repeat-pass interferometry to align the phase centers of two data channels to the same reference path to ensure maximum correlation

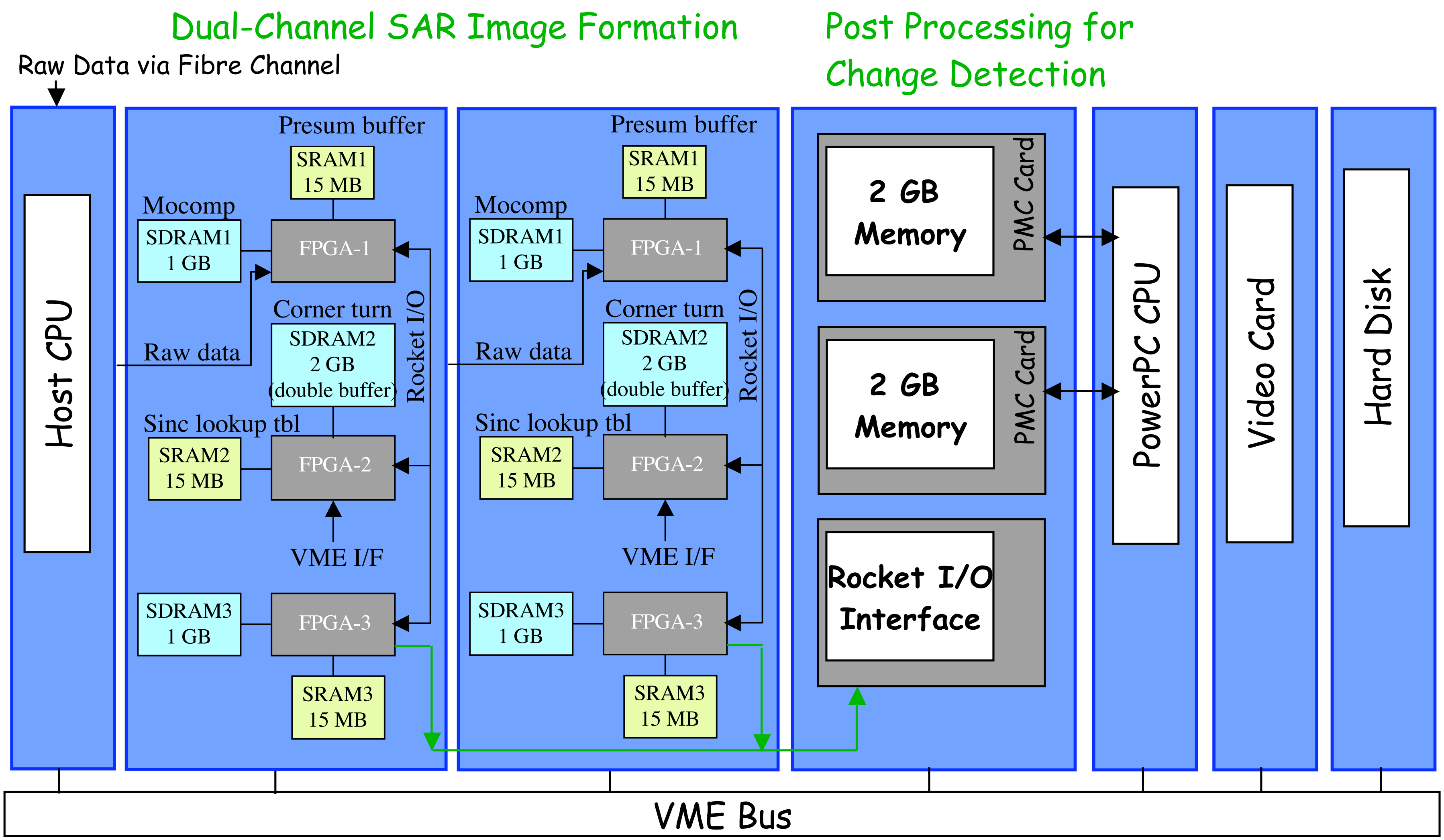


Flow Diagram of Differential Interferogram Formation



* This computationally-intensive step may not be implemented if we run out of resources, in which case we will use a pre-stored interferogram.

Hardware Architecture



Features of Hardware Architecture

- Flexible architecture to provide upgrade path
  - Extra slots in VME chassis to host more data channels
  - FPGAs can be upgraded to accommodate more processing throughput when faster and larger FPGAs become available
- Utilizing the built-in Rocket I/O interface to provide fast (3 Gbps), dedicated data paths between the FPGA cards and the post processor
- Utilizing standard interfaces and COTS hardware whenever possible to minimize cost and development time
- Fibre Channel interface was chosen to input raw data and output processed data for its 2 Gbps data transfer rate and for compatibility with AIRSAR and future UAVSAR's digital systems and with high speed RAID Disks

Status of Processor Development

This 34-month project is funded by NASA Earth Science Technology Office. We are in year 1 of the development effort. We have completed

- Requirements document
- Draft algorithm description document
- Industry survey of signal processing boards and FPGA boards
- Definition of hardware architecture
- Definition of interfaces
- Selection of COTS microprocessor boards
- FPGA design of range compression function

Summary

- Developed an on-board SAR processor architecture for change detection that combines an FPGA front-end with a reconfigurable computing back-end
- Processor architecture will provide optimal performance while maintaining flexibility where needed within the algorithmic implementation
- FPGA development for SAR image formation is underway
- Microprocessor development for change detection will commence in parallel
- We plan to demonstrate the functionality of the on-board processor at the end of year 2